

# **FPGA 2 Specification**

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*64 port G-PON*

**ASGvOLT64**

**(GPON OLT)**

**Version: 1.0**

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## Revision History

| Document<br>Rev. | Date      | Author | Revision Description | CPLD code version |
|------------------|-----------|--------|----------------------|-------------------|
| 1.0              | 8/29/2019 |        | Initial OCP release  |                   |
|                  |           |        |                      |                   |
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### 3.1. Offset 0x01 FPGA version (Read Only)

Example : version 5.01 then reg 0x1 is 5, reg 0x2 is 1

| Bit | Name          | R/W | Reset Value | Description  |
|-----|---------------|-----|-------------|--------------|
| 7:0 | FPGA_ver[7:0] | R   |             | FPGA version |

### 3.2. Offset 0x02 FPGA version (Read Only)

| Bit | Name          | R/W | Reset Value | Description  |
|-----|---------------|-----|-------------|--------------|
| 7:0 | FPGA_ver[7:0] | R   |             | FPGA version |

### 3.3. Offset 0x35 CPLD Uplink LED Stream (Read& Write)

| Bit | Name                  | R/W | Reset Value | Description                         |
|-----|-----------------------|-----|-------------|-------------------------------------|
| 7:6 | Reserved              |     |             |                                     |
| 5   | CPLD3_UPLINK_LED_DATA | R/W |             | Uplink LED DATA from FPGA2 to CPLD3 |
| 4   | CPLD3_UPLINK_LED_CLK  | R/W |             | Uplink LED CLK from FPGA2 to CPLD3  |
| 3   | CPLD2_UPLINK_LED_DATA | R/W |             | Uplink LED DATA from FPGA2 to CPLD2 |
| 2   | CPLD2_UPLINK_LED_CLK  | R/W |             | Uplink LED CLK from FPGA2 to CPLD2  |
| 1   | CPLD1_UPLINK_LED_DATA | R/W |             | Uplink LED DATA from FPGA2 to CPLD1 |
| 0   | CPLD1_UPLINK_LED_CLK  | R/W |             | Uplink LED CLK from FPGA2 to CPLD1  |

### 3.4. Offset 0x35 MAC Uplink LED Stream (Read& Write)

| Bit | Name            | R/W | Reset Value | Description                       |
|-----|-----------------|-----|-------------|-----------------------------------|
| 7:2 | Reserved        |     |             |                                   |
| 1   | UPLINK_LED_DATA | R/W |             | Uplink LED DATA from MAC to FPGA2 |
| 0   | UPLINK_LED_CLK  | R/W |             | Uplink LED CLK from MAC to FPGA2  |

### 3.5. Offset 0x35 CPLD PON LED Stream (Read& Write)

| Bit | Name | R/W | Reset Value | Description |
|-----|------|-----|-------------|-------------|
|-----|------|-----|-------------|-------------|

|     |                    |     |  |                                  |
|-----|--------------------|-----|--|----------------------------------|
| 7:6 | Reserved           |     |  |                                  |
| 5   | CPLD3_PON_LED_DATA | R/W |  | PON LED DATA from FPGA2 to CPLD3 |
| 4   | CPLD3_PON_LED_CLK  | R/W |  | PON LED CLK from FPGA2 to CPLD3  |
| 3   | CPLD2_PON_LED_DATA | R/W |  | PON LED DATA from FPGA2 to CPLD2 |
| 2   | CPLD2_PON_LED_CLK  | R/W |  | PON LED CLK from FPGA2 to CPLD2  |
| 1   | CPLD1_PON_LED_DATA | R/W |  | PON LED DATA from FPGA2 to CPLD1 |
| 0   | CPLD1_PON_LED_CLK  | R/W |  | PON LED CLK from FPGA2 to CPLD1  |



## 4.1. Offset 0x01 System Reset (Read& Write)

| Bit | Name                    | R/W | Reset Value | Description |
|-----|-------------------------|-----|-------------|-------------|
| 7   |                         |     |             |             |
| 6   |                         |     |             |             |
| 5   |                         |     |             |             |
| 4   |                         |     |             |             |
| 3   |                         |     |             |             |
| 2   |                         |     |             |             |
| 1   | JA2_RESETE <sub>n</sub> | R/W |             |             |
| 0   | 82P33914_WPLL_RST       | R/W |             |             |

## 4.2. Offset 0x35 Interrupt Stream (Read& Write)

| Bit | Name                          | R/W | Reset Value | Description                        |
|-----|-------------------------------|-----|-------------|------------------------------------|
| 7   | FPGA1_TO_FPGA2_INTERRUPT_DATA | R/W |             | Interrupt DATA from FPGA1 to FPGA2 |
| 6   | FPGA1_TO_FPGA2_INTERRUPT_CLK  | R/W |             | Interrupt CLK from FPGA1 to FPGA2  |
| 5   | CPLD3_TO_FPGA2_INTERRUPT_DATA | R/W |             | Interrupt DATA from CPLD3 to FPGA2 |
| 4   | CPLD3_TO_FPGA2_INTERRUPT_CLK  | R/W |             | Interrupt CLK from CPLD3 to FPGA2  |
| 3   | CPLD2_TO_FPGA2_INTERRUPT_DATA | R/W |             | Interrupt DATA from CPLD2 to FPGA2 |
| 2   | CPLD2_TO_FPGA2_INTERRUPT_CLK  | R/W |             | Interrupt CLK from CPLD2 to FPGA2  |
| 1   | CPLD1_TO_FPGA2_INTERRUPT_DATA | R/W |             | Interrupt DATA from CPLD1 to FPGA2 |
| 0   | CPLD1_TO_FPGA2_INTERRUPT_CLK  | R/W |             | Interrupt CLK from CPLD1 to FPGA2  |